ABSTRACT OF THE DISCLOSURE

In a 3Tr. NAND including a cell unit constituted of one memory cell and two select gate transistors between which the cell is held, to renew data by a byte unit, at an erase time, a potential of a bit line or source line can be set by the byte unit, so that erase by the byte unit is possible. Accordingly, with respect to only the data of the memory cell which is a renewal object, an erase/write operation is performed, and reliability of a memory operation is enhanced.